B.E. [illegible] Electronics – IC Technology

IC Technology 1/12/16

Q.P. Code : 728402

( 3 Hours ) [Total Marks : 80

N.B. 1) Question No. 1 is compulsory
2) Solve any three questions from the remaining questions
3) Assume suitable data if necessary

1. Solve any four of the following. (5 marks each) (20)
   (a) Explain various charges in the gate oxide after fabrication of MOSFET.
   (b) What is Trench Isolation? Explain its use in VLSI technology.
   (c) Classify crystal structure with respect to resistivity and periodicity of atoms.
   (d) Enlist the steps for obtaining Silicon from Sand.
   (e) Explain Molecular Beam Epitaxy.

2. (a) Define Range, Projected Range and straggle with respect to Ion Implantation. Also explain the damage produced due to light ion and heavy ion with neat diagram. (10)
   (b) Describe APCVD process with neat diagram. Why wafers are lying horizontal in this process. Enlist drawbacks of this process. (10)

3. (a) List out common Unit processes in IC Fabrication. What is the difference between N-well and P-well process? Draw final cross-sectional view of CMOS inverter fabrication using N-well process with appropriate labels? (10)
   (b) Draw layout of CMOS inverter along with its circuit diagram. Mention clearly all dimensions as per lambda rules. Explain buried and butting contact. (10)

4. (a) Explain Steps of Lithography with suitable diagrams. Also classify Lithography techniques. (10)
   (b) What is SOI technology? Enlist methods for fabrication of SOI. Explain any one of it. (10)

5. (a) Describe with the help of a neat diagram Hayness-Schokley experiment for measurement of Drift Mobility of n-type semiconductor. (10)
   (b) Compare evaporation and sputtering methods for metal deposition. Which methods are commonly used for deposition of Silicon, $SiO_2$ and metals? (10)

6. Write short notes on any four of the following. (5 marks each) (20)
   (a) Parametric test and functionality test for IC testing
   (b) Electric package reliability.
   (c) Silicon Crystal defects
   (d) Multiagte device Structures
   (e) MESFET fabrication process

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