BE - sem - VII (old) ETRX - VLSI Design
15/12/16

Q.P. Code : 630501

Time:-3 Hrs **Marks: 100**

N.B. : 1. Question one is compulsory
2. Solve any four out of remaining six questions
3. Draw neat diagrams
4. Assume suitable data if required.
5. Symbols have their usual meanings.

Q. 1.	A) Draw and explain VTC of CMOS inverter.	
	B) Explain diffusion process.	
	C) Explain lambda based design rules	
	D) Explain the necessity of HDL	20
Q. 2	A) Draw and explain fabrication steps of CMOS inverter.	10
	B) Draw mask layout for two input CMOS NOR gate.	10
Q. 3	A) Explain epitaxial process.	10
	B) Explain implementation of ripple carry adder.	10
Q. 4	A. Explain constant voltage scaling in detail.	10
	B. Derive equations for Noise margin for CMOS inverter.	10
Q. 5	A. Write Verilog programe for full adder using two half adders.	10
	B. Differentiate between semi-custom and full-custom devices.	10
Q. 6	A. Explain various short channel effects.	10
	B. Realize Y=(A+B)(C+D) using CMOS technology.	10
Q.7	Write short notes on following	20
	A. VLSI design flow	
	B. VLSI design rules	
	C. Buried contact	
	D. Depletion load inverter	

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