

S.E. ETRX sem III CBGS Nov-13 25/11/13

Ash5-D:\Data-35

Sys- Electronics Devices

Con. 7851-13.

GX-12037

(3 Hours)

[Total Marks : 80

N.B. : (1) Question No. 1 is compulsory and solve any three questions from remaining questions.

(2) Assume suitable data if necessary.

(3) Draw neat and clean figures.

Given Data :-

$$q = 1.6 \times 10^{-19} \text{ C}$$

$$k = 1.38 \times 10^{-23} \text{ J/K}$$

$$\eta_i = 1.5 \times 10^{10} \text{ cm}^{-3}$$

$$\epsilon_{si} = 11.7 \times 8.854 \times 10^{-14}$$

1. (a) Justify that the space charge width increase with reverse biased voltage in a p-n junction diode. 5
- (b) Sketch low frequency capacitance versus gate voltage of a MOS capacitor with n-type substrate show individual capacitance components. 5
- (c) Sketch the IV characteristics of a PN junction solar cell. 5
- (d) Describe construction and V-I characteristics of IGBT. 5
2. (a) Derive equation of built in potential V_{bi} for a p-n junction under Zero bias and hence calculate V_{bi} at $T = 300 \text{ K}$ for $N_d = 10^{15} \text{ cm}^{-3}$ and $N_a = 10^{15} \text{ cm}^{-3}$. 10
- (b) What is primary advantage of HBT over BJT? Draw and explain schematic cross section of an npn HBT structure with its energy band diagram when HBT is operated under active mode? 10
3. (a) Explain construction and V-I characteristics of Tunnel diode. 10
- (b) Explain construction, working and characteristic of N-channel JFET, explain frequency limitation factors. 10

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4. (a) Draw band diagrams for accumulation, depletion and inversion regions for MOS capacitor. 10
 Calculate threshold voltage for a polysilicon gate n-channel MOS transistor with substrate at Zero potential with the following parameters :-
 Substrate doping density $N_A = 10^{16} \text{ cm}^{-3}$
 Polysilicon gate doping density $N_D = 2 \times 10^{20} \text{ cm}^{-3}$
 Gate oxide thickness $t_{ox} = 500 \text{ \AA}$
 Oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$
- (b) Describe the time delay factors in the frequency limitation of the bipolar transistor, calculate the emitter-collector transit time, cut off frequency and the beta cut off frequency of a bipolar transistor, with the following parameters, consider a silicon npn transistor at $T = 300 \text{ K}$ with a low frequency common emitter current gain of $\beta = 100$. Assume the following parameters :- 10
 $I_E = 50 \mu\text{A}$, $C_{je} = 0.40 \text{ PF}$, $C_{\mu} = 0.05 \text{ PF}$
 $X_B = 0.5 \mu\text{m}$, $D_n = 25 \text{ cm}^2/\text{s}$, $X_{\text{ac}} = 2.4 \mu\text{m}$
 $r_c = 20 \Omega$, $C_s = 0.1 \text{ pF}$
5. (a) Describe construction, working and characteristic of :- 10
 (i) Photodiode and
 (ii) Avalanche Photodiode.
- (b) Discuss the device structure and principle of operation of MESFET. Derive the equation for current-voltage characteristics for MESFET. Describe the various regions of operation on V-I characteristics. 10
6. (a) Explain construction, working and characteristics of SCR. 10
- (b) Explain the need of Hetero junction, explain the terms straddling, staggered and broken gap in relation to hetero junction. Explain the quantization of energy of an electron in a potential well in hetero junction. Explain this concept with respect to the ideal energy band diagram of an nN GaAs-Al GaAs hetero junction in thermal equilibrium. 10
