30/11/2015 BE SEM VII - EIX -- CBGS - ICT

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N.	В.		Subjects.com	QP Code: 5901	
	1)	Question No. 1 is compulsory		Time: 3 Hours.	
	2)	Solve any three questions from remaining quest	tions	Max. Marks: 80	
	3)	Assume suitable data if necessary			
1.	Solve any four of the following			(20)	
	(a)	Explain predeposition and drive in steps in diffusion	process.		
	(b)	Classify and discuss in brief the types of Thin Film D	eposition methods.		
	(c)	What is Hall effect? Enlist important electrical parameters for which measurement is			
		required before device processing begins.			
	(d)	Explain the need of isolation in VISI and list the methods to accomplish it?			
		Explain SOI fabrication using bonded SOI and	ATTENDED TO CONTRACT CONTRACT OF A PRINCIPAL PRINCIPAL	a2zSubjects.com	
2.	101	Displant our moneauth achig conduct our min	Sinari out motilou.	·	
	(2)	Explain Czochralski method for Silicon crystal growt	th What are its disasta	(10)	
	100 E	Explain Czochralski method for Silicon crystal growth. What are its advantages? (10) What do you mean by Class of a clean room? Give the steps in a standard RCA cycle during			
	(2)	wafer cleaning			
		water cleaning	, T	(10)	
2					
3.	1-1	a) Evaluin Solid source diffusion system with post discrete Alexander and a second of the second of			
	(a)	Explain Solid source diffusion system with neat diagram. Also give one example of each			
	62 Carlo	source for P-type and N-type diffusion.		(10)	
		Explain High K and Low K dielectrics with application		(05)	
	(c)	What are the basic reactions in formation of SiO ₂ in dry oxidation and wet oxidation?			
		Explain where these methods are used during MOS	FET fabrication process	. (05)	
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4.		u225u5jeeisieom			
	(a)	Explain the fabrication process steps along with vertical cross-sectional views for CMOS			
	40.1120	inverter using N-well process		(10)	
	(b)	What are the different types of design rules? Draw		ANGESTICAL DESCRIPTION OF THE PROPERTY OF THE	
_		lambda (λ) based design rules (Show units in lambd	ia).	(10)	
5.					
	(a)	Enlist important electrical parameters for which me			
		processing begins. Also describe the experimental s resistivity measurement with the help of a neat dia	CONTRACTOR OF THE PROPERTY OF	method for (10)	
	(b)	Explain the difference between SOI Finfet and bulk		(03)	
•	0.000	State advantages of Finfet devices over single gate		A A TABLE POWER	
sectional views of different multigate structures. a22				(07)	
6.	Wr	te short notes on any three of the following	a2zSubjects.com	n (20)	
	(s)	MESFET Fabrication			
	(6)	Carbon Nanotube Transistor			
· N		SOI Technology			
	(d)	Parametric tests and Functionality tests for IC testing	ng		