

SELEXTCL III CBGS 28/5/14

D E

QP Code :NP-18690

(3 Hours)

[Total Marks : 80]

- N.B.**
- (1) Question No. 1 is **compulsory**.
 - (2) Out of remaining questions, attempt any **three** questions.
 - (3) Assume suitable additional data if **required**.
 - (4) Figures in brackets on the right hand side indicate **full marks**.

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| 1. Explain the following :- | 20 |
| (a) For ECL and CMOS logic families define- | |
| (i) noise margin (ii) fan-in (iii) fan-out. | |
| (b) Compare Asynchronous and synchronous counter | |
| (c) Explain static RAM | |
| (d) Explain Master-Slave J.K Flip-flop. | |
| 2. (a) Perform following operation using 2's compliment method- | 5 |
| (i) $(28)_{10} - (42)_{10}$ (ii) $(52)_{10} - (-18)_{10}$ | |
| (b) Prove the following using Boolean algebra. | 5 |
| $\overline{A}BC + A\overline{B}C + ABC + A\overline{B}\overline{C} = AB + BC + CA$ | |
| (c) Design 2 bit comparator. | 10 |
| 3. (a) Minimize the following using Quine Mc Clusky method. | 10 |
| $F(A, B, C, D) = \Sigma m(3, 4, 9, 13, 14, 15) + \Sigma d(5, 6)$ | |
| (b) Design synchronous counter using J. K flip-flop for the given sequence — | 10 |
| 0 – 2 – 3 – 5 – 7 – 0. | |
| 4. (a) Design following Boolean equation using 4 : 1 mux | 5 |
| $F((A, B, C, D) = \Sigma m(2, 4, 5, 7, 9, 11, 12)$ | |
| (b) Compare EEPROM and FLASH memories. | 5 |
| (c) Explain bidirectional 4 bit universal shift register. | 10 |
| 5. (a) Explain 3 : 8 decoder. | 5 |
| (b) Explain Mealey machine and Moore machine. | 5 |
| (c) Write VHDL code for 3 bit binary down counter. | 10 |
| 6. (a) Explain Architecture and features of FPGA. | 10 |
| (b) Implement Ex-OR gate using NAND | 5 |
| (c) Convert $(118)_{10}$ in to (i) BCD (ii) Hexadecimal (iii) octal. | 5 |