CMOS VLSI Design

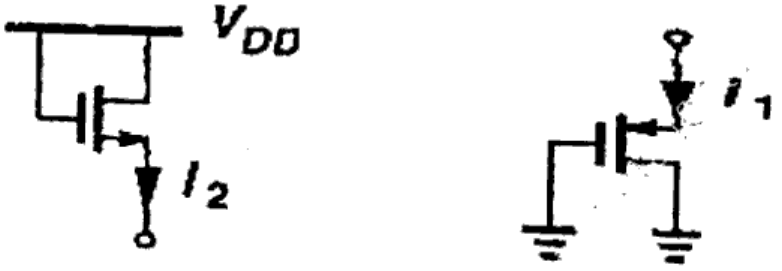
Sem-VIII (CBSGS) ETRX - C'MOS VLSI D

Q.P. Code : 719702

(3 Hours) [Total Marks : 80

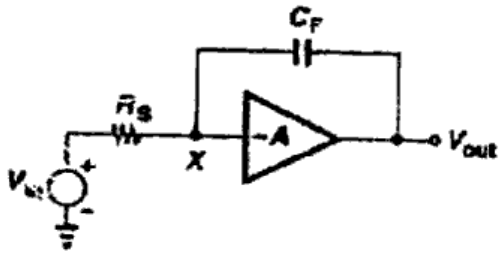
N.B. : (1) Question **ONE** is **compulsory**.
(2) Solve **any THREE** out of remaining **questions**.
(3) Draw **neat** and **clean diagrams**.
(4) Assume **suitable data** if **required**.

1. (a) Will the following circuits work as current sources? Give the correct reason for your answer.



(b) List down the performance parameters of VCO and explain trade off between them. 5

(c) Calculate the pole associated with the node X shown in the following figure. Assume $R_S = 1K\Omega$, $C_F = 0.1pF$ and $A = 10$. 5

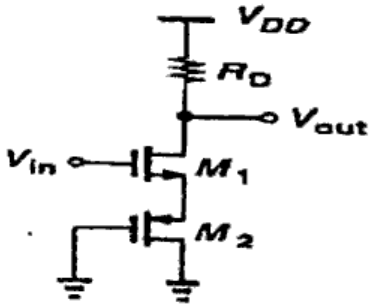


(d) Draw and explain the floor plan for a possible mixed signal chip. 5

2. (a) Show the op-amp based implementation of temperature independent bandgap reference and various issues involved thereof. 10

(b) For common source stage with diode connected load, if the variation of $\eta = (g_{mb}/g_m)$ with the output voltage is neglected then prove that the gain is independent of bias currents and voltages. 5

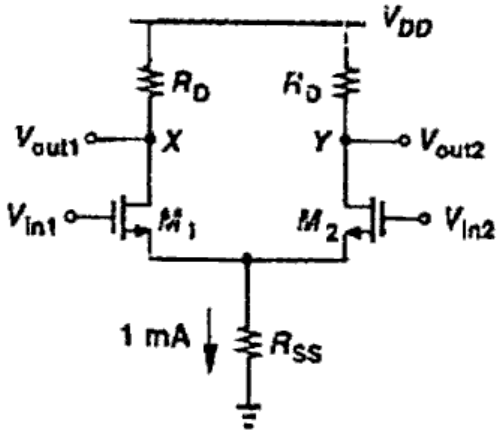
(c) Assuming $\lambda = \gamma = 0$, calculate the small signal gain of the circuit shown: 5



3. (a) The following circuit shown in Figure uses a resistor rather than a current source to define a tail current of 1mA. Assume $(W/L)_{1,2} = 25/0.5$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$ and $V_{DD} = 3$V. 10

(a) What is the required input CM for which Rss sustains 0.5V?

(b) Calculate R_D for a differential gain of 5.



(b) Explain the concept of switched capacitor circuit. Draw and explain discrete time integrator along with the output waveform. 10

4. (a) With the use of small signal behaviour, prove that for differential pair the magnitude of differential gain is equal to $g_m R_D$ regardless of how the inputs are applied. 10

(b) What is the need of compensating operational amplifiers? Explain the compensation of two stage operational amplifiers? 5

(c) Derive an expression for the input referred noise voltage of common source stage. 5

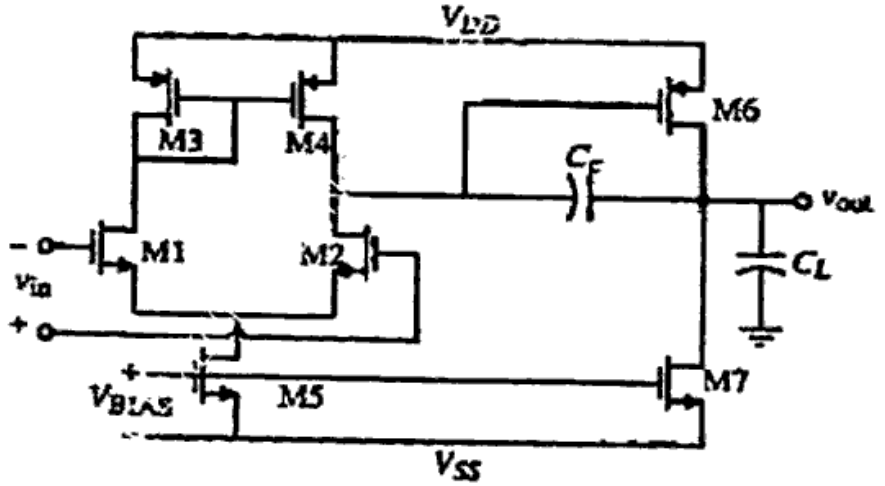
5. (a) Design two stage Operational Transconductance Amplifier (OTA) similar to that shown in the figure to meet the following specifications with a phase margin of 60° : 15

$A_v > 5000$ V / V $V_{DD} = 2.5$ V $V_{SS} = -2.5$ V
Gain Bandwidth (GB) = 10MHz $C_L = 10$pF
Slew Rate (SR) > 10 V/μs V_{out} range = ± 2.5 V
ICMR = −1 to 2 V $P_{diss} \leq 2$ mW

Use the following table for material and device parameters. Assume $C_{ox} = 2.47$ fF/μm².

Parameter	n - channel	p - channel	Unit
V_{TO}	0.7 ± 0.15	−0.7 ± 0.15	V
K'	110	50	μA/V²
λ	0.04	0.05	V⁻¹

Verify that the voltage gain and power dissipation given in the specifications are met by the designed circuit.



(b) Explain charge-pump PLL.

6. (a) Compare the performance of various op-amp topologies.
(b) Explain the input-output characteristics of phase detector (PD) circuit. 5
(c) Explain the concept of clock feedthrough. 5
(d) Compare between full-custom and semi-custom design. 5