

Sem-III / Digital Electronics. / INST / 14-05-15

QP Code : 4845

(3 Hours)

[Total Marks : 80

- N.B. (1) Question no. 1 is compulsory
 (2) Attempt any three questions from the remaining
 (3) Assume suitable data if necessary.
1. Solve:- 20
- (a) Prove that $L.(M + \bar{N}) + \bar{L}.\bar{P}.\bar{Q}. = (L + \bar{P}.Q)(\bar{L} + M + \bar{N})$
- (b) Implement $f(ABC) = \sum m(1, 2, 5)$ using 4:1 mux.
- (c) Compare synchronous and asynchronous counter.
- (d) What is race around condition? How to avoid it?
2. 5
- (a) Design half adder using logic gates 5
- (b) Convert in standard SOP form, $y = AB + BC + AC$ 10
- (c) For the given logical equation,
 $F = AB + AC + C + AD + ABC$ 10
- (i) Design k-map
- (ii) Express in standard SOP equation.
- (iii) Minimize and realize the above equation using NOR gate only.
3. 10
- (a) Realize the following using 16: 1 MUX and only one 8: 1 MUX 10
- $f(A, B, C, D) = \sum m(2, 3, 5, 7, 9, 11, 15)$
- (b) What is shift register? Explain the working of 4 bit bidirectional shift register. 10
4. 10
- (a) Convert JK Flip to T-Flip flop and D-Flip Flop 10
- (b) Design 4 bit Binary to Gray code converter. 10
5. 10
- (a) Design MOD-6 synchronous counter using JK Flip Flop 10
- (b) Design 4-bit BCD Adder using binary adder IC 7483 10
6. Write note on (any four):- 20
- (a) De Morgan's Theorem
- (b) Noise margin and fanout digital Ic's
- (c) PAL and PLA
- (d) ALU
- (e) Priority encoder
- (f) Johnson counter.

JP-Con. 8893-15.